

WE CLAIM:

1. A semiconductor device including a bonding pad having  
interconnecting metallization protected by an  
5 insulating layer, said metallization selectively  
exposed by a window in said insulating layer,  
comprising:
  - a patterned seed metal layer positioned on said  
interconnecting metallization exposed by said  
10 window and overlapping a portion of said  
insulating layer around said window;
  - a metal stud on said seed metal, said stud aligned  
with said window, said stud including a top  
surface and side surfaces;
  - 15 a barrier metal layer conformally covering the top  
and side surfaces of said stud; and
  - an outermost bondable metal layer over said barrier  
metal layer.
2. The device according to Claim 1 wherein said outermost  
20 metal layer conformally covers said barrier layer and  
provides a flat surface having an average roughness of  
less than about 50 nm.
3. The device according to Claim 1 further comprising a  
bond wire attached to said outermost metal.
- 25 4. The device according to Claim 1 wherein said  
interconnecting metallization comprises copper.
5. The device according to Claim 1 wherein said seed metal  
layer comprises copper.
6. The device according to Claim 1 wherein said seed metal  
30 layer comprises a stack of a refractory metal layer and  
a copper layer.

7. The device according to Claim 1 wherein said insulating layer is selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbide, silicon dioxide, polyimide, or stacked layers thereof.
- 5 8. The device according to Claim 1 wherein said metal stud comprises copper.
9. The device according to Claim 1 wherein said barrier layer comprises nickel.
10. The device according to Claim 1 further comprising an  
10 additional barrier layer positioned between said barrier layer and said outermost layer, said additional barrier layer comprising palladium.
11. The device according to Claim 1 wherein said outermost bondable metal layer comprises gold.
- 15 12. A method for fabricating a semiconductor device having interconnecting metallization protected by an insulating layer, said metallization selectively exposed by windows in said insulating layer, said method comprising the steps of:  
20 depositing a conductive seed layer to cover said metallization exposed by said window and to cover a portion of said insulating layer around said window;  
forming a metal stud over said conductive seed metal  
25 layer covering said metallization exposed by said window and over said portion of said insulating layer around said window, said metal stud including a top surface and side surfaces;  
removing said conductive seed layer portions not  
30 covered by said metal stud;  
conformally covering said top and side surfaces of said metal stud with a barrier metal; and

depositing an outermost bondable metal layer over  
said barrier layer.

13. The method according to Claim 12 wherein said outermost layer conformally covers said barrier layer and  
5 provides a surface having an average surface roughness of less than about 50 nm.
14. The method according to Claim 12 further comprising the step of attaching a bond wire to said outermost metal layer.
- 10 15. The method according to Claim 12 wherein said interconnecting metallization comprises copper.
16. The method according to Claim 12 wherein said seed layer comprises copper.
17. The method according to Claim 12 wherein said seed  
15 layer comprises a stack of a refractory metal layer and a copper layer.
18. The method according to Claim 12 wherein said metal stud comprises copper.
19. The method according to Claim 12 wherein said step of  
20 forming said metal stud comprises forming said stud using electrolytic plating.
20. The method according to Claim 12 wherein said barrier metal comprises nickel.
21. The method according to Claim 12 wherein said step of  
25 depositing said barrier metal comprises depositing said barrier metal using electroless plating.
22. The method according to Claim 12 further comprising the step of depositing a second barrier metal layer to conformally cover the first barrier layer, the metal of  
30 said second barrier layer selected to resist diffusion of said first barrier metal.

23. The method according to Claim 22 wherein said second barrier metal comprises palladium.
24. The method according to Claim 22 wherein said step of depositing said second barrier metal comprises  
5 depositing said second barrier metal using electroless plating.
25. The method according to Claim 12 wherein said outermost metal layer comprises gold.
26. The method according to Claim 12 wherein said step of  
10 depositing said outermost metal comprises depositing said outermost metal using electroless plating.
27. The method according to Claim 12 wherein said step of depositing a conductive seed layer is preceded by a step of cleaning and etching the surface of said wafer,  
15 comprising the steps of:
- exposing said wafer to an organic solvent, thereby removing organic contamination and mechanical particles from said exposed metallization, and drying said wafer;
- 20 exposing said wafer in a vacuum chamber to an oxygen and nitrogen/argon/helium plasma, thereby ashing any organic residue on said exposed metallization and oxidizing the metal surface to a controlled thickness; and
- 25 exposing said wafer to a hydrogen and nitrogen/helium/argon plasma without breaking the vacuum of said chamber, thereby removing said controlled metal oxide from said window surface and passivating said cleaned surface, creating a  
30 fresh and activated surface.